



N-Channel 2.5-V (G-S) MOSFET

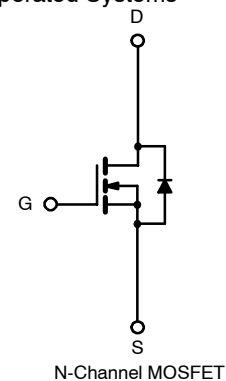
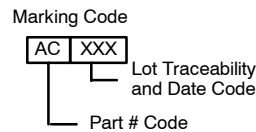
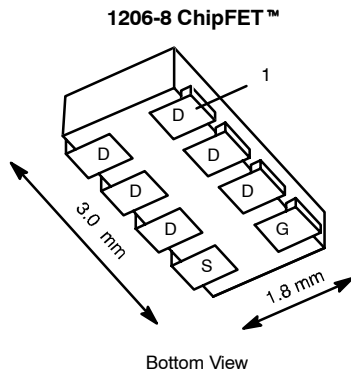
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
12	0.020 @ $V_{GS} = 4.5$ V	9.5
	0.025 @ $V_{GS} = 2.5$ V	8.5

FEATURES

- TrenchFET® Power MOSFETs: 2.5-V Rated
- Low Thermal Resistance

APPLICATIONS

- Load/Power Switching for Cell Phones and Pagers
- PA Switch in Cellular Devices
- Battery Operated Systems



Ordering Information: Si5406DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	12		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	9.5	6.9	A
	$T_A = 85^\circ\text{C}$		6.8	4.9	
Pulsed Drain Current		I_{DM}	20		
Continuous Source Current (Diode Conduction) ^a		I_S	2.1	1.1	W
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	1.3	
	$T_A = 85^\circ\text{C}$		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	40	50	$^\circ\text{C}/\text{W}$
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)		R_{thJF}	15	20	

Notes

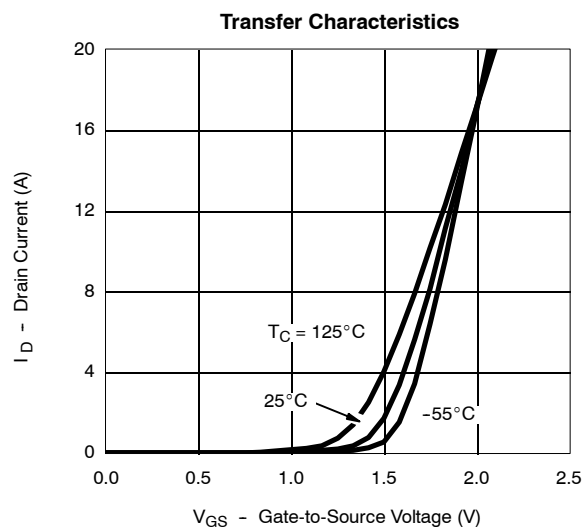
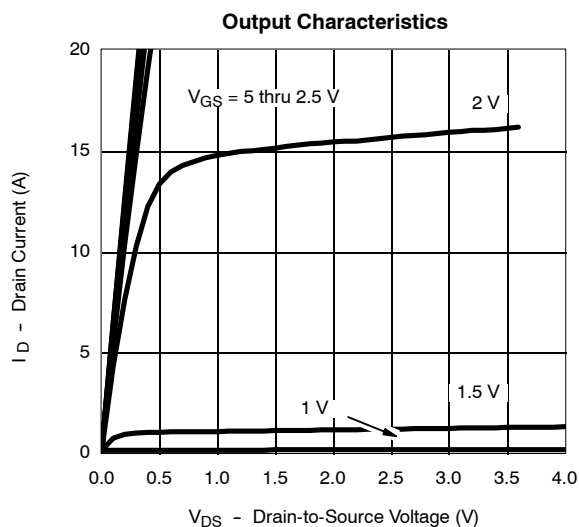
- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1.2 mA	0.6			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 9.6 V, V _{GS} = 0 V			1	μA
		V _{DS} = 9.6 V, V _{GS} = 0 V, T _J = 85 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 6.9 A		0.017	0.020	Ω
		V _{GS} = 2.5 V, I _D = 2 A		0.021	0.025	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 6.9 A		30		S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.1 A, V _{GS} = 0 V		0.7	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 6.9 A		13.7	20	nC
Gate-Source Charge	Q _{gs}			2.3		
Gate-Drain Charge	Q _{gd}			4.1		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		17	25	ns
Rise Time	t _r			46	70	
Turn-Off Delay Time	t _{d(off)}			54	80	
Fall Time	t _f			29	45	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.1 A, di/dt = 100 A/μs		35	70	

Notes

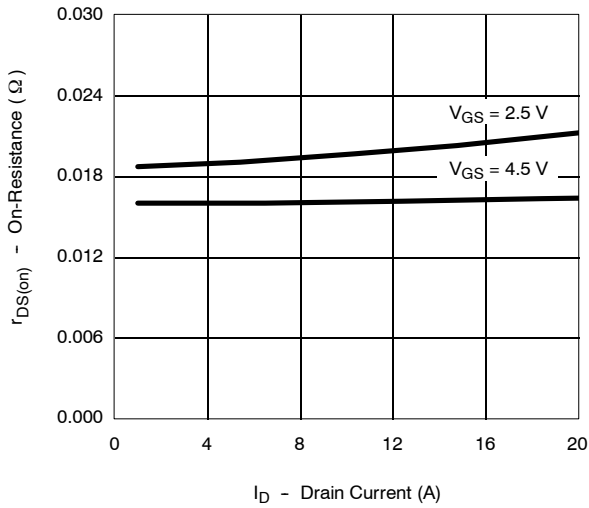
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

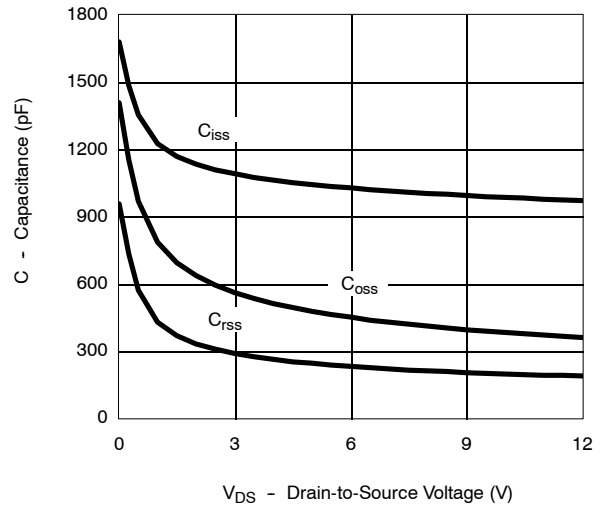


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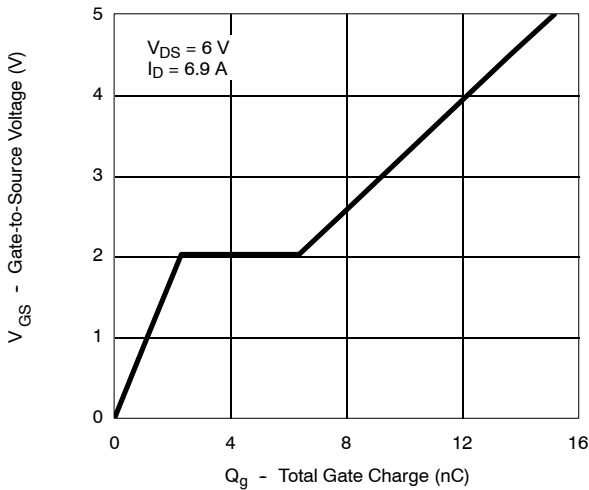
On-Resistance vs. Drain Current



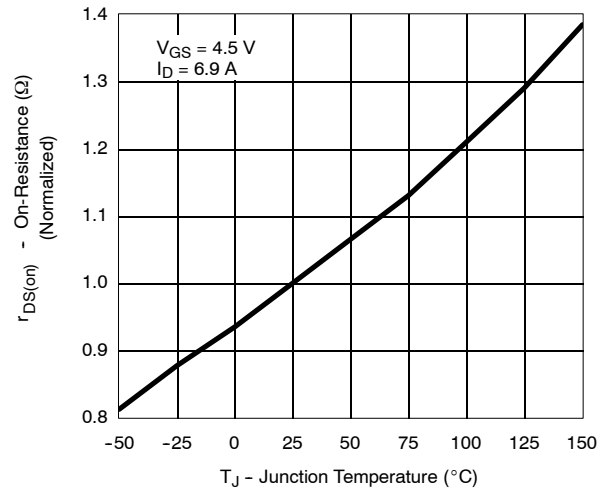
Capacitance



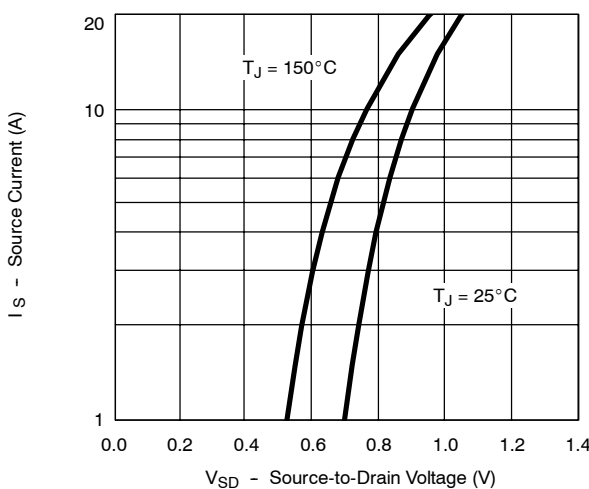
Gate Charge



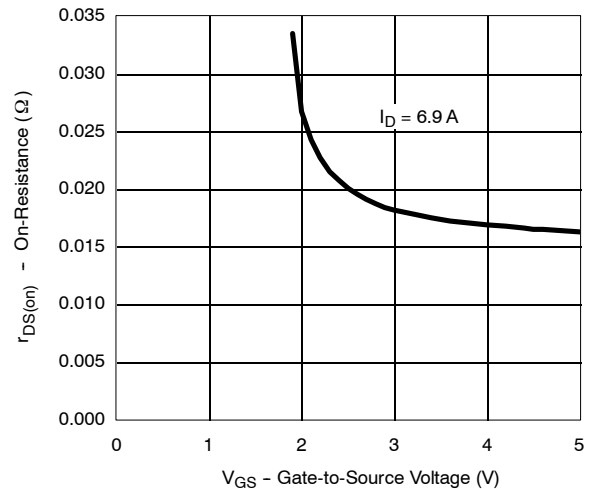
On-Resistance vs. Junction Temperature



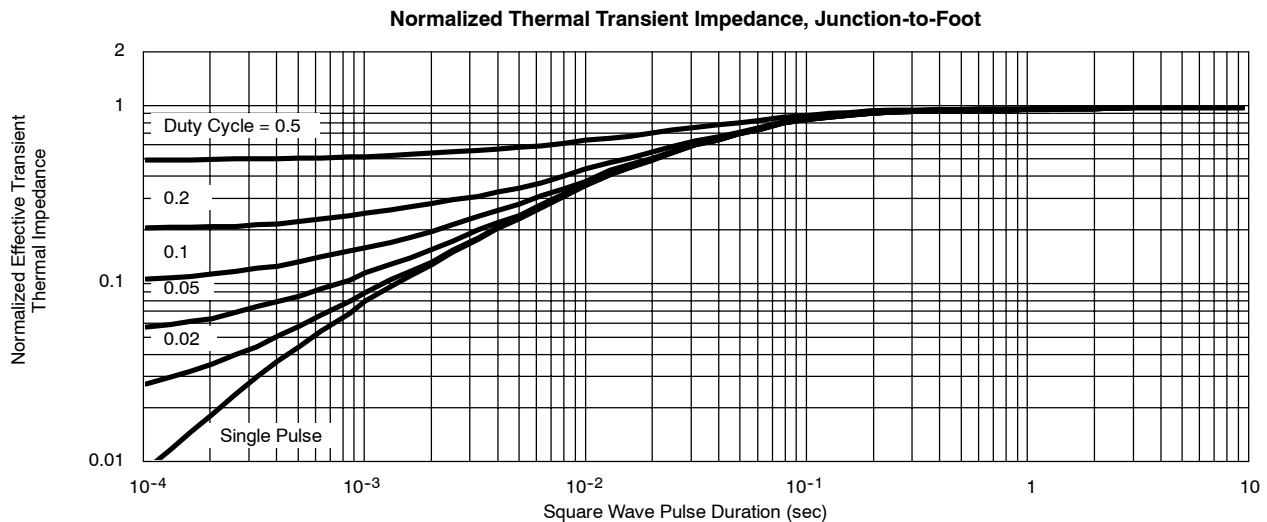
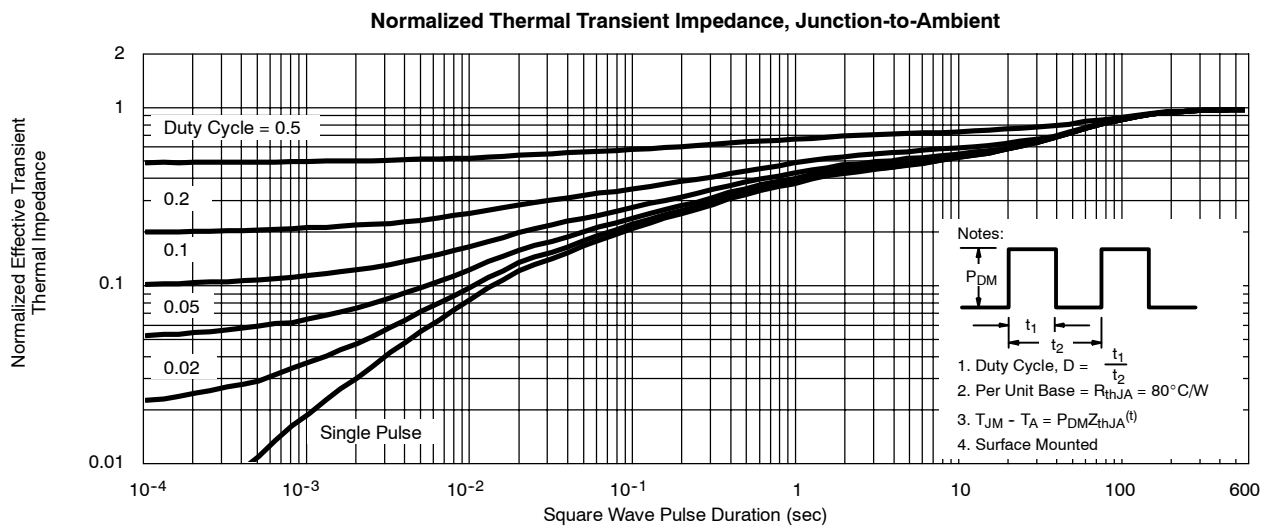
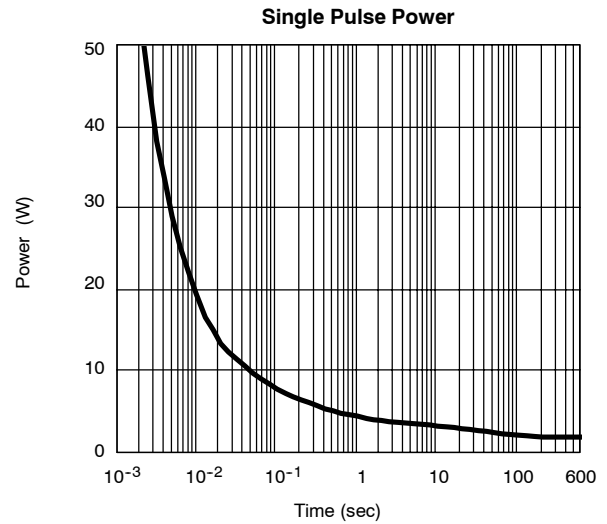
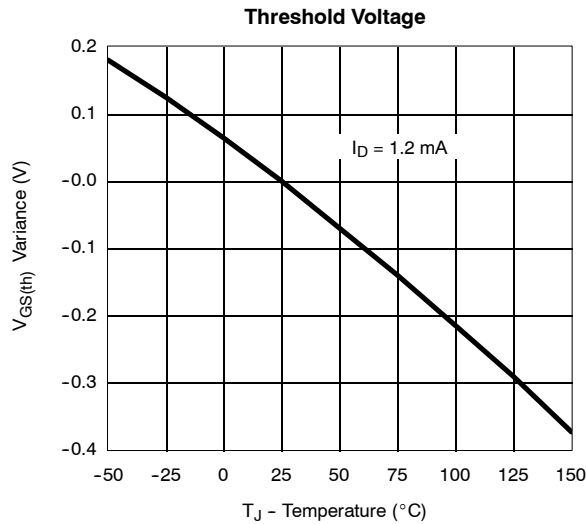
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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